

AUG 10 2005

**Fax transmission from:**

U.S. Naval Research Laboratory
Associate Counsel Intellectual Property, Code 1008.2
4555 Overlook Avenue, SW
Washington, DC 20375-5325

From: Joe Grunkemeyer

Phone: (202) 404-1556

Fax: (202) 404-7380

Date: 08/10/2005**To:** Examiner Kevin D. Mew

Art Unit 2664

Fax: (571) 273-8300

Cover Sheet + 3 Pages**Message:**

RE: Patent Application No.: 09/715,778

Filed: 11/17/2000

Inventor: Dennis

Docket No.: NC 84,779

Response to Final Rejection – 3 pages

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PATENT APPLICATION
Docket No.: NC 84,779

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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AUG 10 2005

In the application of: Dennis

Serial No.: 09/715,778

Filed: 11/17/2000

For: PRIORITIZING RESOURCE UTILIZATION IN MULTI-THREAD COMPUTING
SYSTEM

Examiner: Mew, Kevin D.

Art Group Unit: 2664

Honorable Commissioner of Patents
PO Box 1450
Alexandria, VA 22313-1450

August 10, 2005

RESPONSE TO FINAL REJECTION

Sir:

In response to the Office action of 06/10/2005, setting a three month shortened statutory period of reply, please consider the following remarks.

Claims 1-30 are pending in the application. No claims are presently allowed.

Claim Rejections – 35 U.S.C. § 102

Claims 1-30 have been rejected under 35 U.S.C § 102(e) as allegedly anticipated by Blueloch et al. (UP 6,434,590).

Claim 1, as amended, is to a processor capable of simultaneous execution of two or more threads of instructions. The processor comprises at least one resource unit, a priority register, and a priority selector. The resource unit is capable of being assigned to two or more of the threads. The priority register stores thread information for the threads including a priority code corresponding to each thread. The priority selector generates an assignment signal to assign the resource unit to the requesting thread according to the priority codes.

CERTIFICATE OF FACSIMILE TRANSMISSION

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8/10/05
Date

Joseph T. Grunkemeyer
Joseph T. Grunkemeyer

Serial No.: 09/715,778

PATENT APPLICATION
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Blelloch discloses a system and method of parallel processing. An assignment manager assigns tasks to a system of processing elements. Each processing element has a computation element CE and a memory element ME. Each computation element can access each memory element (col. 3, lines 9-18).

In order to make a *prima facie* case of anticipation, the reference must disclose each limitation of the claim. Blelloch does not disclose the limitation that at least one of the threads requests use of the resource unit. The thread is a series of instructions, some of which require the use of a resource. When such an instruction is encountered, a resource is requested. The request is triggered by the thread.

The Examiner stated that the system of processing element SY1 of Blelloch corresponds to the processor of the present claim 1, that a processing element PE corresponds to one thread of instruction execution, and that the router RT1 corresponds to the resource unit of the present claim 1 (Office Action of 06/10/2005, page 10, lines 1-13). However, the processing element does not correspond to the thread. The processing element is hardware, and the thread is software being executed on hardware. The thread of claim 1 requests a resource unit when it contains an instruction that requires the resource unit to execute the instruction (p. 10, lines 5-9). However, the processing element requests the router to receive tasks from the assignment manager (col. 2, lines 47-51). The processing element request is not triggered by an instruction within a thread, but depends upon the ability of the processing element to receive another task. Blelloch does not disclose a thread containing a request to use the router.

Claims 11 and 21 are method and processor claims containing the limitations of claim 1, and claims 2-10, 12-20, and 22-30 depend from and contain the limitations of claims 1, 11, and 21, respectively. These claims are asserted to distinguish from the reference in the same manner as claim 1.

In view of the foregoing, it is submitted that the application is now in condition for allowance.

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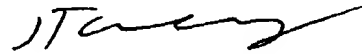
Serial No.: 09/715,778

PATENT APPLICATION

Docket No.: NC 84,779

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Respectfully submitted,



Joseph T. Grunkemeyer

Reg. No. 46,746

Phone No. 202-404-1556

Office of the Associate Counsel

(Patents), Code 1008.2

Naval Research Laboratory

4555 Overlook Ave, SW

Washington, DC 20375-5325